

REMARKS

Claims 1-24 remain pending in the reissue application.

In the Office Action mailed March 24, 2009, the Examiner rejected claims 1-24 under 35 U.S.C. § 251 on the grounds the rejected claims were based on “lack of reissuable” error.

In remarks accompanying the rejection, the Examiner stated: (1) the preamble was ignored because it was a mere statement of purpose, (2) the changes to the claims were “of no substance in changing the limitations of the initial claims set,” and (3) the statement identifying errors in the application is “in essence without meaning since the claims limit to a neural network notwithstanding the use of the term ‘neural’ in the preamble.”

Applicants respectfully disagree and request reconsideration and further examination of the claims.

Claim Preamble

The Examiner asserts that the use of the word “neural” in the preamble is essentially a “mere statement of purpose,” and that applicants did not provide any comments why MPEP § 211.02II would not apply.

Applicants submit that the use of the word “neural” in the preamble is unnecessarily limiting because it provides a descriptive limitation on the word “network.” In other words, the word “neural” is used as an adjective to modify the type of network that is being claimed. Applicants have recognized that the circuits provided in the disclosure have applications outside of the neural arena. For example, the last sentence in the first paragraph under the Summary of the Invention states that the “present invention has been to focus on circuits” in which very little power per connection is consumed. Also stated in the same paragraph is that the flexibility and power consumption of the hardware implementation satisfies “a wide range of applications.”

In the first and second paragraphs of the Detailed Description, applicants describe the present invention as using a single pair of flash-EEPROM devices for both analog storage and analog computation. The inventive concept was identified as making use of “a floating-gate

device as a programmable switched conductance.” The use of the pair of transistors allows for differential input, increasing the functionality both within the neural signal processing and in areas outside of neural networks.

Moreover, with respect to the description of Figure 4C, applicants describe one of the concepts “underlying the present invention is to make use of conductance summing for performing computation and for converting an analog-valued conductance signal into a binary-valued output signal suitable for communication.” The circuit 5 is identified both as a “neuron” and as a “neuron circuit” in the description.

Thus, the circuit in the disclosure is described both in terms of a neural network and in terms of the hardware electrical circuit, *i.e.*, transistors and a conductance summing circuit.

The use of the word “neuron” in the preamble can be construed to limit the network circuit to that of the neural type, as discussed above. Because applicants recognize that the circuit of the present invention has applications outside of the neural field, applicants desire the claims to not be limited to just neural networks and neural applications.

Neuron Stage Limitation

The Examiner further indicated that removal of the limitation “neuron stage coupled to the synaptic weighting elements” in claims 7 and 13 did not remove any limitation because, in the Examiner’s view, the neuron stage was described in the specification as merely functioning as a comparator.

However, a “neuron stage” includes more than just a comparator. The “neuron stage” provides not only for measuring conductance on the basis of current through the memory cells, it also generates a binary output signal on the basis of the total conductance of the synaptic elements. (See abstract, last sentence.) In fact, it is the comparing stage 5 that is identified as a “neuron,” and not as a neuron stage. Hence, by removing the limitation “neuron stage” from the claim and reciting only a comparison circuit, the claim in essence is broadened because only a comparator circuit is claimed and not the entire stage.

Identification of Error

The Examiner asserts that the initial claim set characterized a neural network without the recitation of “neural” in the preamble and, thus, the applicants’ statement is, in essence, without meaning as to the identified error since the claims limit to a neural network notwithstanding the use of the term “neural” in the preamble.

However, several of the claims in the reissue application do not use the word “neural” or “neuron” or the words “neuron stage” in both the preamble and the body of the claims. For example, claim 23 is directed to a system having a plurality of synaptic weighting elements, a conducting sensing circuit, and a latch stage coupled to the conducting sensing circuit to digitize the output signal. Claim 17 is similarly directed to an analog circuit that does not use the words “neuron,” “neural,” or “neuron stage.” The same is true for the claim set starting with independent claim 13 and ending with dependent claim 15. Claims 7-9 are likewise void of the use of these words.

Conclusion

Although the Examiner asserts that the elimination of the word “neural” is of no consequence, at least with respect to patentability, applicants are also concerned with enforceability. Unnecessary verbiage in a claim can lead to enforcement failures when the claims are parsed by a court and jury. In the present case, applicants’ claims have been reviewed by experts and found to be potentially unnecessarily limiting due to the use of the “neural” and “neuron” verbiage in the claims.

In view of the foregoing, applicants respectfully submit that the present reissue application adequately identifies a reissuable error, and that the claims identified above are patentably distinct from the initial claims that issued.

In view of the foregoing, applicants respectfully submit that all of the claims presented in this reissue application are in condition for allowance. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Application No. 10/631,323
Reply to Office Action dated March 24, 2009

All of the claims remaining in the application are now clearly allowable.
Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
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